LEWICKI
microelectronic fe
forschung + entwicklung

LEWICKI Allee 35 Postf. 20 D-7931 Oberdischingen b. Ulm W.-Germany

Integrierte Dick- u. Dünnfilmschaltungen
Mikroelektronische Baugruppen
Entwicklung von Prototypen
Serienfertigung
Beratung

Circuits intégrés
à couches minces et couches épaisses
Blocs d'assemblage microélectroniques
Développement de prototypes
Fabrication en série
Ingénieur - Conseil

Thick and thin film Integrated Circuits
Microelectronic subsystems
Custom designed prototypes
Production
Consulting Engineeres

The European Space Research and
Technology Centre
Domeinweg
Noordwijk, Netherlands

Ihr Zeichen Your reference	Ihre Nachricht Your letter of	Unser Zeichen Our reference	Datum Date
			JULY 1978

Ref.: Call for competitive offer no. AO/987/NL/HP

Subject:

Design, development and testing of a hybrid thick film memory package.

Telefon (07305)-6588 u. 5588 | Telex 0712355 lew d | Bank Raiffeisenbank Oberdischingen Kto. 585800006 (BLZ 63069972), Dresdner Bank Ulm Kto. 8150539 (BLZ 63080015)

ESTEC CONTRACT No. 2119/73 hp
Sous-Contrat No. D6/GB/NO 1675
INTERTECHNIQUE - LEWICKI

Rapport Technique

PACKAGING D'UNE MÉMOIRE À SEMI-Conducteur

Technologie Hybride Avancée
Étude d'Avant-Projet

HYBRID-ICs
LEWICKI Micro-electronic
SPACE-PACKs

First Report: SURVEY OF SEMICONDUCTOR COMPONENTS MOUNTING AND PACKAGING TECHNOLOGIES

A) SURVEY OF SEMICONDUCTOR COMPONENTS MOUNTING AND PACKAGING TECHNOLOGIE

1. Interconnecting Substrate Systems
1.1. Conventional (Plastic) Multilayers
1.2. Conventional (Plastic) Mini - Multilayers (MICAPLY)
1.3. Composite Substrate
1.4. Thickfilm Ceramic Multilayers
1.4.1. Thickfilm Materials
1.4.1.1 Normal oxidizing (air) Atmosphere firing Pastes
1.4.1.2. The Molybdenum- and Titanium-Mangnese Process (reducing atmosphere firing)
1.4.1.3. New Reactive Cu, Ni, Al Pastes
1.4.1.4. Aluminum Thickfilm Metallization
1.4.1.5. Resin Based Thickfilm Pastes
1.4.1.6. Photolithographic Thickfilm Pastes
1.4.1.7. Substrate Materials
1.5 Thin Film Circuits
2. Patterning Techniques
2.1. Screen printing Masks
2.2. Photo-Etching
3. Double Side Multilayer Multichip Substrates

APPENDIX

B) LITERATURE REFERENCES/SOURCES

1. Applicable official Standards and Specifications
2. Books
3. Articles + Lectures
4. Other references

c) TERMS AND DEFINITIONS

Second Report: SEMICONDUCTOR COMPONENTS (Packaging Types, Handling, Test)

A. SEMICONDUCTOR COMPONENTS

1. Survey of available Semiconductor Components

1.1. Preencapsulated Chips

1.1.1. Hermetic Mini - Packages

1.1.2. Plastic Mini - Packages

1.2. Unencapsulated Chips

1.2.1. Conventional Chips

1.2.2. Beam Lead Chips

1.2.3. Flipchips

1.2.4. Spider Chips and others

2. Selected Semiconductor Components

2.1 Types, Physical and Technological Data of the Semiconductor Supplier

B. LARGE (CMOS) CHIPS HANDLING, TESTING, STORAGE

1. Large IC Chips Handling and Protection
2. LEWICKI antistatic CMOS Laboratory
3. Mounting Considerations for CMOS Chips
4. CMOS Chip Handling, Bonding, Testing, Operation
5. Storing of CMOS Chips
6. Handling of unmounted CMOS Chips
7. Handling Hybrid CMOS ICs and Subassemblies
8. Automatic Handling Equipment for CMOS Chips
9. Electrical Failure Modes due to improper Handling

Third Report : OPTIMIZATION OF SUBSTRATE COMPLEXITY AND PACKAGING CONCEPT

A OPTIMIZATION OF SUBSTRATE COMPLEXITY

1. Reasons for maximum Complexity
1.1 Reliability
1.1.1 External Substrate Interconnections
1.1.2 Shock and Vibration Resistance

1.2 Volume and Weight
1.3 Component Manufacturing Costs
1.4 Speed and Cut Off Frequency
1.5 Equipment Design, Production, Time of Repair

2. Reasons for Minimum Complexity
2.1 Substrate Yield
2.1.1 Unrepairable, nonredundant Substrates
2.1.2 Yield Increase By Selection and Repair
2.1.3 Yield Increase by Redundanay and Auto-Repair
2.2 Technological Restrictions
2.3 Internal Substrate Interconnection Patterns
2.4 Equipment Repair Materials Costs
2.5 Flexibility in Substrate Application
2.6 Power Dissipation and heat transfer

3. Comparison Chart
4. Optimization of Substrate Complexity
4.1 Power Dissipation Optimum
4.2 Harness Minimization
(optimal Equipment Circuit Partition)
4.3 Versatility and Flexibility
4.4 Testing, Maintenance, Repair
4.5 Costs
4.5.1 Component Costs
4.5.2 Equipment Costs
5. Result

Third Report (cont'd)

B. OPTIMIZATION OF SUBSTRATE SIZE

1. Main Chip Interconnection Systems
1.1 Prepackaged single Chips
1.2 Unencapsulated conventional chips
1.3 Beam Lead Chips, Flip Chips etc.

2. Main hybrid Substrate Concepts
2.1 Unencapsulated Chips on uncased Substrates
2.2 Unencapsulated Chips on cased Substrates
2.3 Prepackaged Chips (Flatpacks) on uncased Substrates

3. Optimization of Chip Density (Adhesive Tolerances, Chip Dislocation, Wire loop length, Thickfilm Conductor Density, Cap Sizes)

4. Optimization of Substrate Sizes
4.1 Substrate with uncased chips
4.2 Substrates with Flatpacks T091

5. Substrate Interconnection Systems
5.1 Fexible PCBs for Substrate Interconnection
5.2 V-Jumpers
5.3 Hook + Eye
5.4 Hook + Bus
5.5 Pin + Jack, Jack + Bus
5.6 Multy-Substrate Packaging System MSPS7310
5.7 Light-Weight Substrate Support System

6. Substrate Support Systems
6.1 Multy-Substrate Packaging System MSPS 7310
6.2 Light-Weight Substrate Support System

4 th Report : SELECTED THICKFILM PROCESS

A) SELECTION OF SUITABLE THICKFILM PROCESSES

1. General
2. Selection criteria
2.1 Qualification Standard
2.2 Reliability
2.3 Heat dissipation
2.4 Volume, weight
2.5 Versatility and Flexibility
2.6 Testing, Maintenance, Repair
2.7 Logistics and Availability
2.8 Economics
2.9 Conclusion

3. Selected Thickfilm Process A
3.1 General
3.2 Process Flow chart and QA Plan
3.3 Reasons for the selection

4. Selected Process B
4.1 General
4.2 Process flowchart and QA Plan
4.3 Reasons for the selection

B Technologies worth watching

1. The Beam Lead process
2. Fotosensitive Thickfilm Pastes

C Excluded Technologies

1. Flipchips (with balls, bumps, pillars)
2. Organic Multilayer(e.g. Micaply)
3. Plastic Thickfilms

D Quality Assurance Plan

Fourth Report (cont'd)

E CRITICAL PROCESS ELEMENTS AND PARAMETERS

1. Direct Chip to Chip wiring
2. Double sided Multichip Substrates
3. Substrate Testing befor packaging
3.1 Optimized Layout for defective Chip Detection
3.2 Defective Chip Detection Test
3.3 Defective Chip Detection Technology and Tooling
3.3.1 Superclean, antistatic, inspectabel Test Setup
3.3.2 Micromanipulated fast microprobe
3.3.3 Disconnection of wires
3.3.4 Shorting by wire loops or conductive advesive brid
4. Repair Techniques
4.1 Chips on Substrate
4.2 Wires on Substrate and Chips
4.3 Substrates in Box
5. Chip Protection
5.1 Hermetic and non hermetic Chip "Caps"
5.2 Protective Resin Drop Material (space grade)
6. Substrate Size and Thickness Optimization
7. Vibrabion and Shock Stability
8. Substrate Mounting Techniques
9. Light-Weight cubic Memory Box Technology
10. Hermetic (glass sealed) Feed Throughs
11. Hermetic Sealing of Box (soldering, welding)
12. Pressure and Thermal-Vacuum Tests
13. Repair of the sealed Box

Fifth Report: PROPOSAL FOR AN OPTIMIZED ADVANCED SEMICONDUCTOR MEMORY

A) OPTIMAL HYBRID MEMORY SYSTEMS

1. CMOS System
1.1 Advanced Concept AC1
1.2 Advanced Concept AC2
1.3 Advanced Concept AC3
1.4 State of the Art Concept BC
1.5 Conventional Concept CC
1.6 Comparison Chart

2. PMOS and CCD Systems
2.1 2 clock Circuits per Substrate
2.2 4 clock Circuits per Substrate

3 CMOS-PMOS Comparison Chart

4. Discussion
5. Hybrid Manufacturers Choice
6. Future Validity of the advanced semiconductor memory

B) HYBRID TECHNOLOGIES TO BE WATCHED

1. Beam Lead
2. Fotosensitive Thickfilms

C) RELIABILITY CONSIDERATIONS

1. Environmental Conditions
2. Chip Level
3. Hybrid Substrate Level
4. Substrate Pile Level
5. Complete Memory Unit Level

D) IMPORTANCE OF REPARABILITY

1. Yield, Redundancy and Autorepair
2. Chip Level
3. Hybrid Substrate Level
4. Substrate Pile Level
5. Complete Memory Unit Level

Fifth Report, cont'd.

E) SUPPLIER/CUSTOMER FLOW CHART AND INTERFACES

F) RESPONSIBILITIES AND WARRANTIES

1. General
2. Circuit Design Level
3. Chip Level
4. Hybrid Substrate Level
5. Substrate Pile Level
6. Complete Memory Unit Level

G) OPTIMAL TIME TO START PHASE 2 (DEVELOPMENT)

TABLE OF CONTENT

1. Technical Description of Hardware
1.1 Description of Hybrid Development and Fabrication
A. Manufacturing Flow Plan
B. Description of Thickfilm Manufacturing Process
C. Optimization of Substrate Size
D. Substrate Interconnection Systems
E. Quality Assurance Flow Plan
F. General Hybrid Fabrication Plan and QA-organization
1.2 Functional Description of the proposed CMOS Memories
1.3 Description of the Technical Options to be developed

2. Flow Chart of the Program and its Work Breakdown

3. Work Package Description

4. Cost Plans
4.1 Costplan of the 64kbit Memory Option
4.2 Costplan of the 144kbit Memory Option

5. Program Schedule

6. Key Personnel

7. Facilities

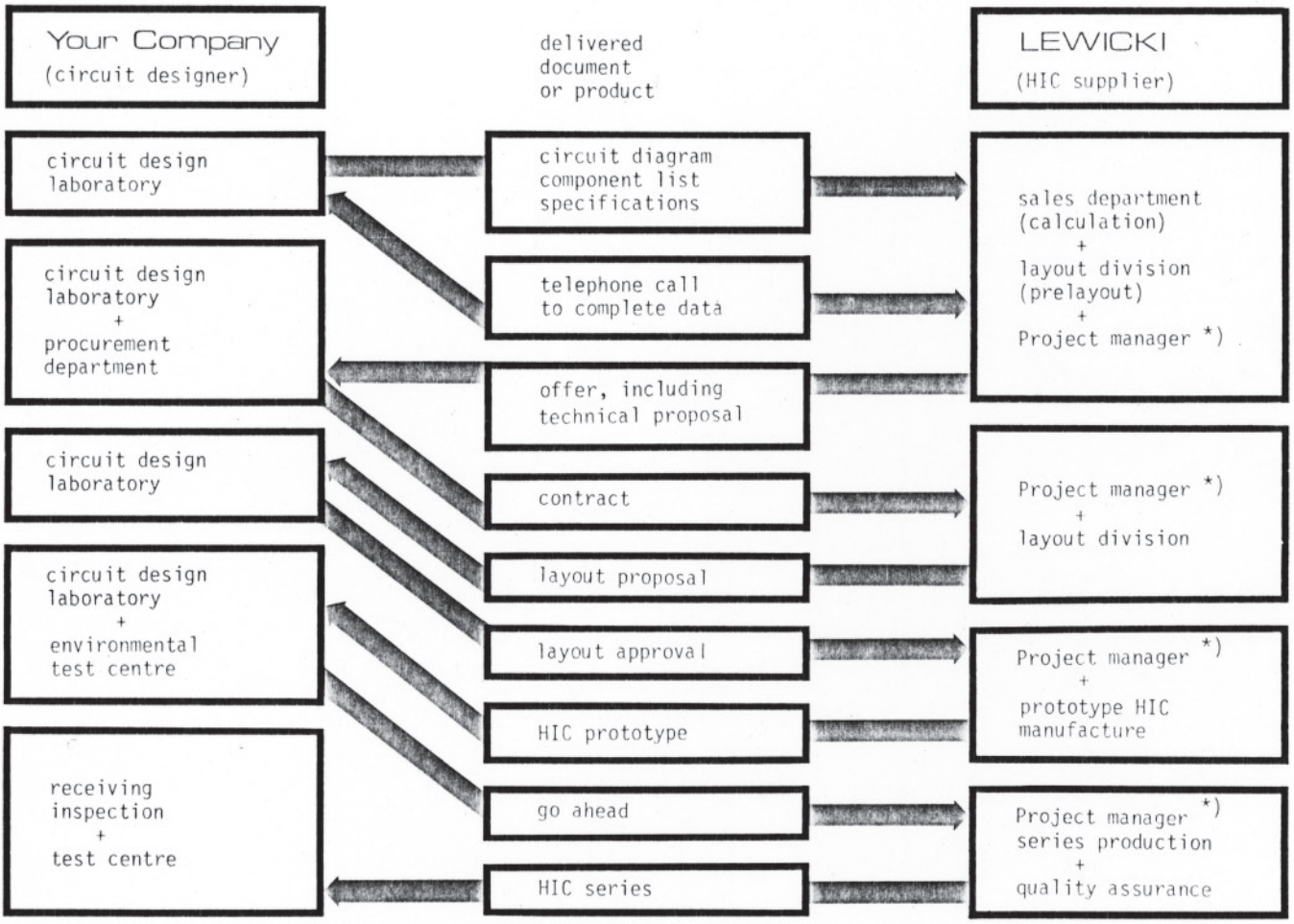
8. Experience of the Tenderer Organization and his Consultants

1. TECHNICAL DESCRIPTION OF HARDWARE

1.1 Description of hybrid development and fabrication

A) MANUFACTURING FLOW PLAN / PROCESS USED FOR THICKFILM MANUFACTURE

FLOW CHART



*) he will act as Your representative at LEWICKI

B) DESCRIPTION OF THICKFILM MANUFACTURING PROCESS

In addition to the enclosed thickfilm manufacture flow chart the following description is given:

1. Substrates
   Generally 96% Al_2O_3 alumina substrates are used, beside of 99,9% Al_2O_3, glassivated alumina and beryllium-oxide BeO for maximum heat dissipation.
   Before use the substrates are 100% tested on shock resistance, vibration and bending strength, roughness and flatness and surface density (by coloured liquids).

Acoustical sound analyzation is one of the test methods. Sample lots are tested on paste adhesion (peel, pull), resistive paste sheet resistance and other parameters destructively.

2. Conductors

Prefered are the Pt, Pd, Au and other noble metals bearing conductive pastes to be fired in oxygene atmosphere. Because of complete elimination of silver migration problems, silver and silver palladium pastes are not normally applied. Conductive patterns are made by screen printing with stainless steel screens or polyamid screens, both with indirect or direct-indirect masks and also with contact/ off contact printing, where the resolution of the screen-printing process is sufficient.

For better resolution (microwave, micristrip, beam lead) fotolithographic etching techniques are applied.

The hydrogen atmosphere (or wet ammonia) firing conductive paste systems especially Molybden-Manganese and Moly-Titanium are employed where extremly high adhesion strength is importand (hermetical sealing, brazing leads at high temperatures) or special etching, electroplating or barrel plating (Ni, Au etc.) technologies are necessary.

3. Resistors

Only the best inks are used, with TCR from 30 ppm/^{o}C to 150 ppm/^{o}C in the normal range of sheet resistivity and to 250 ppm/^{o}C over 10 MOhm/square or under 10 Ohms/square. Most belong to the platinum-ruthenium group. Special firing cycles (time, temperature, atmosphere) have been developed for low TCR, low noise, high voltage-, temperature- and time stability (aging).

Trimming is commonly done with a company owned process, which eliminates the microscratches, fissures and aging causing erosive sand blasting. Laser trimming is available but because of other disadvantages on the resistor qualities seldom in use (only for very small, not too narrow tolerated resistors).

Our investigations have shown, that our trimming process gives higher resistor long time and temperature stress stability to the resistors as other processes do.

4. Dielectrics

For ceramic multilayer circuits we prefer the glass-ceramics dielectrics which polycrystallize at temperatures irreversibly under their resoftning point.

Thus large number of layers can be fired successivly without damaging the earlier fired ones.

The same dielectrics with higher epsilon are used because of their higher electrical strength for capacitors.
Protective layers over resistors are the low melting glasses, sometimes coloured for indication.

5. Other Pastes

NTC, VDR, Cds fotosensitive and semiconductive layers, ferrits, black optoelectronic layers, glass solders for hermetic sealing, solder/resin pastes for discrete pretinning and reflow soldering, resin based conductive resistive and dielectric coatings and adhasives and many other materials are successfully employed in our production to solve special space electronic problems.

6. Component Type

In high-rel electronics until now we mostly employ hermetically sealed semiconductors (metal, ceramic or glass packages) which are qualified by NASA (QPL), ESTEC or GfW or which are qualified according to MIL-STD-883, if the customer agrees.
An importand progress to higher reliability, lower weight and volume started with the introduction of beam lead devices. These eliminates half of the critical thermocompression or ultrasonic bonds and carry an "integrated hermetic package", of zero volume. It is the additional silicon-nitrid layer which stops ion migration and "channeling", so that the beam lead semiconductor devices can exist with the same or higher level of reliability without bulky, critical to seal packages as the conventional, unprotected chips need. But with our experience we able to solve this problem with unprotected chips as well. Attention has to be given carefully to the facts of handling and testing of these components.
Capacitors of the multilayer type with COG (=NPO) or W5R (=K1200) ceramics are used where possible. We are convinced, that unencapsulated (but ceramic covered) chipcapacitors are electrical and mechanical better suited as the resin packaged and molded types are.
For all incorporated components prevision is given to the compensation of expansion differences to the substrate. This mounting techiques are importand if environmental temperatures under $-25^{o}C$ exist or when temperature stress cyclings produce strong temperature gradients.

7. Encapsulation, Terminals and Interfaces

The thickfilm modules can be mounted directly on a ceramic or epoxy printed circuit board in similar ways as Dual-in-line or flatpack packages are mounted and interconnected.

Where outgassing is not too critical, additional acidfree silicon adhesive or rubber with primer are successfully in use to mount the substrate to the mother-board. Leads are mechanical connected with the substrates through holes and there soldered and brazed. Thus the electrical contact is not mechanically stress-ed (shocks, vibration, weight). Leads are flexible enough to follow thermal or mechanical differences between module and substrate.
For better protection two substrates can be mounted together to form a SPACE-PACK(R), with the discrete components between. This technique is described on pages 11E and 12E of "ELECTRONICS", Sept.1., 1969. It is applied for patent and since severall years produced for high-rel aerospace electronics.

C) OPTIMIZATION OF SUBSTRATE SIZE

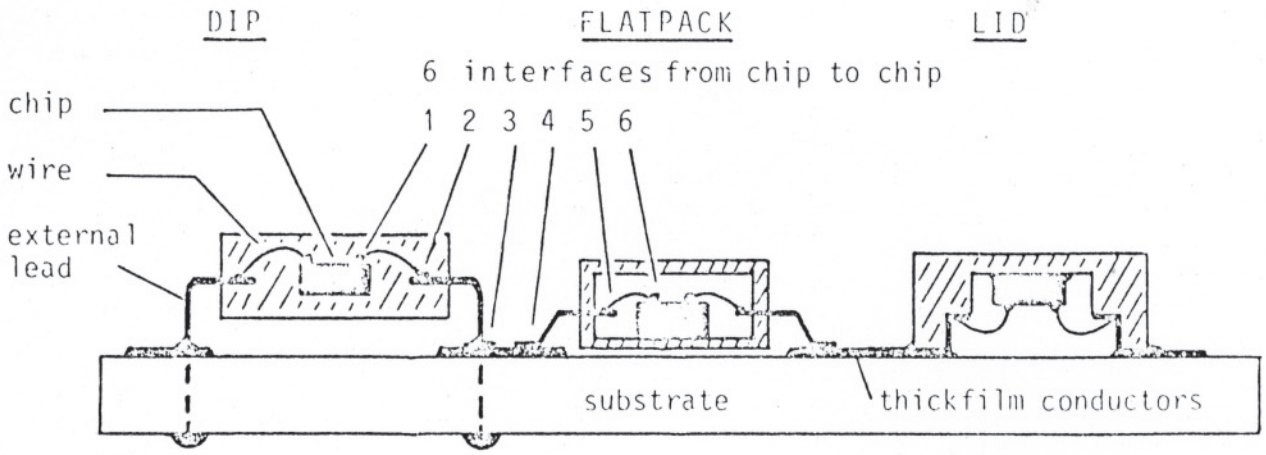
1. Main Chip Interconnection Systems

Figures a), b) and c) show the 3 main levels on which the semiconductor devices can be interconnected by conductive substrate systems (e.g. PCB or ceramic substrate).

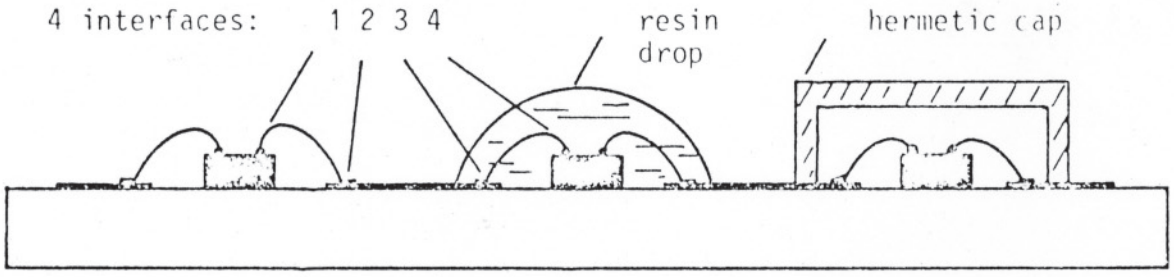
In figure a) the interconnection is done on the level of individual prepackaged semiconductor devices (e.g. Dual-in-line packages, "Leadless-Inverted-Devices"(LIDs) or flatpacks TO84).
Here 6 interfaces have to be reliably bonded to connect one chip electrode pad to the pad of another chip.

If unencapsulated conventional chips are directly bonded to the substrate (fig. b) only 4 interfaces need to be bonded, wiring from chip to chip.
This means an important increase in reliability.
Also the direct chip mounting needs less chip handling and thus less probable damage.

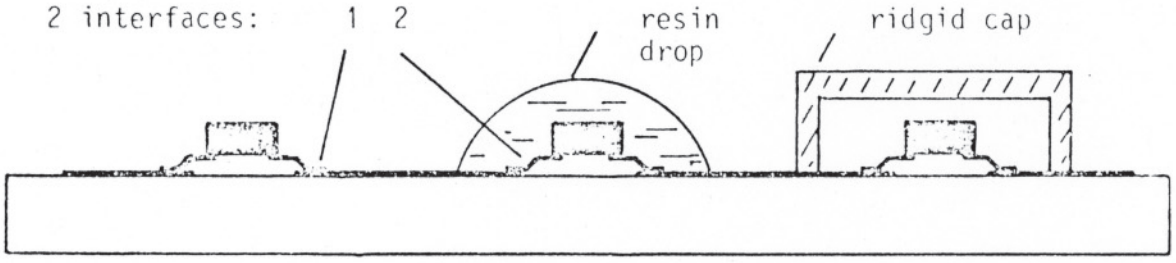
The highest level of reliability possible today is achieved when beam lead divices (class B and A) are used (fig. c.). Their external gold leads reduce the number of necessary bonds from chip to chip down to 2 or to 33 % as compared with prepackaged devices.



a) Prepackaged Single Chips
Soldered or welded to the common interconnecting substrate (e.g. plastic multilayer boards or thickfilm ceramic multilayer).
6 interfaces from chip to chip. Lowest reliability level.



b) Unencapsulated conventional chips
directly bonded to the common interconnecting substrate. Individual and/or common protective resin cover or hermetic cap.
4 interfaces from chip to chip. Medium reliability level.

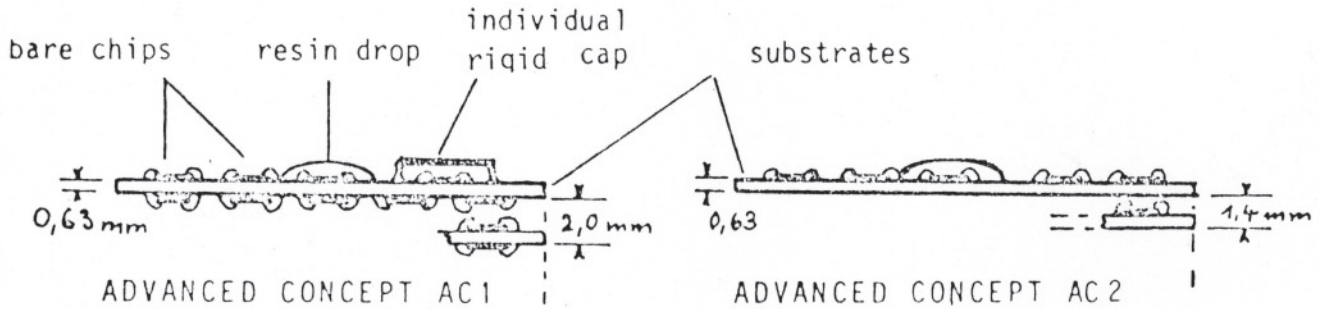


c) Beam Lead chips
have their own external leads. Only one bond per lead is necessary to connect them to the common substrate.
Only 2 interfaces from chip to chip. Highest reliability level.

2. Main hybrid Substrate Concepts

Figures AC1, AC2, AC3, BC and CC show the main hybrid substrate concepts which can be considered to be favorable in packaging.

Structures, advantages and disadvantages of these main substrate concepts are described in table 3, "Hybrid Substrate Comparison Chart".

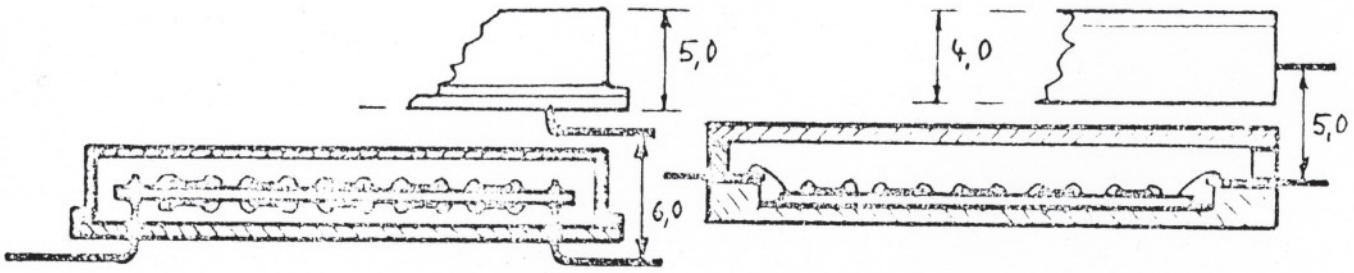


ADVANCED CONCEPT AC1

double side uncased substrates in common box

ADVANCED CONCEPT AC2

single side uncased substrates in common box

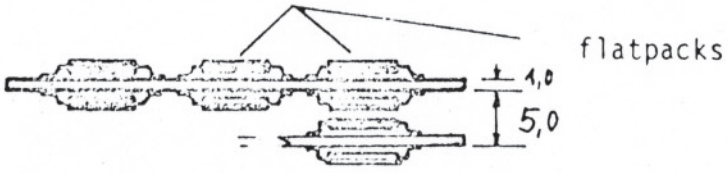


ADVANCED CONCEPT AC3

double side substrates in individual packages

STATE OF THE ART CONCEPT BC

single side substrates in individual packages



CONVENTIONAL CONCEPT CC

chips prepackaged in conventional hermetic packages (e.g. flatpacks)

TABLE 3 Hybrid Substrate Comparison Chart

	Advanced Concept AC1	Advanced Concept AC2
General	non-preencapsulated chips are directly mounted to both substrate sides. Chips are individually protected by resin drops or ridgid caps. All uncased substrates are mounted within the common hermetic metal memory box.	non-preencapsulated chips are directly mounted to one single substrate side. Chips are individually protected by resin drops or ridgid caps. All uncased substrates are mounted within the common hermetic metal memory box.
Advantages	Smallest volume and weight (about 1/7 of that with prepackaged chips as with concept CC). High reliability because low number of internal bonds. Lower chip costs. No substrate package costs	Similar low volume as AC1 (only 1/6 of CC) and only 30 % of the weight of CC (but double the weight of AC1). No investigation of the double side technology necessary. Lower development and production costs than AC1 and lower chip and packaging costs as AC3, BC,CC. Less interconnections than CC.
Disadvantages	Certain (dynamic) chip tests and burn-in can be done only after chips have been mounted. This makes more chip exchanges necessary. Substrates must be carefully handled until inserted into common box.	Double the weight and double the number of substrates to be handled compared with AC1; in addition the disadvantages of AC1.

	Advanced Concept AC 3	State of the Art Concept BC
General	non-preencapsulated chips are directly mounted to both substrate sides. Chips are protected by the hermetic package of each individual substrate.	non-preencapsulated chips are directly mounted to one single substrate side. Chips are protected by the hermetic package of each individual substrate.
Advantages	only half the volume (but the same weight) of CC. The packaged substrates can be handled without danger the chips. Also the substrates may be sent from the manufacturer to the equipment producer without protection. Less interconnections than with CC (higher reliability).	No double side technology necessary (less costs). Less interconnections than with CC (higher reliability).
Disadvantages	relative procurement, test and burn as for AC1. Higher packaging costs than for AC1 and AC2. After sealing of the packages no repair is possible (total substrate lost if one single chip fails)	No gain in weight and volume as compared with CC (prepackaged chips). Weight even 75 % more than with CC. No substrate repair possible after package has been sealed (see AC3).

	Conventional Concept CC
General	preencapsulated chips in hermetic metal or ceramic miniature packages (flatpacks etc., flexible leads preferred) are soldered to both sides of the substrate. The substrates are mounted without further protection within the common metal memory box.
Advantages	Easy procurement, tests and burn in of semiconductor components. Less repair on substrates. As compared with packaged substrates of AC3+BC individual ICs may be exchanged for substrate repair.
Disadvantages	largest volume (8 times that of AC1) and one of the highest in weight. Most complex interconnections system because of the additional leads of the individual chip packages.

3. Optimization of Chip Density

The distance between 2 adjacent chips should be as small as possible to minimize substrate size and weight, but it must be large enough to prevent conductive or nonconductive MOS chip adhesives to cause shortings between thickfilm conductors or to cover them so that wire bonds cannot be made.
Also chip spacings must be sufficient to allow the necessary spacings between thickfilm conductors themselves and to avoid contact of wire loops during shock and vibration.

Minimal chip spacings are 2 to 2,5 mm at the present state of the art.
But with these spacings it is no more possible to lead thickfilm interconnections between the wire lands in the upper conductive layer. In most cases 3 instead of 2 conductive layers will be necessary for the considered memory circuitry.

This means a cost encrease of 30 % to 50 % for development and per substrate as well.
For cost reduction 3 mm to 6 mm chip clearance are optimal.

For pre-encapsulated chips (Flatpacks, LiD etc.) 5 mm to 8 mm are normal where external ribbon leads extent the package.
Between lead free package sides a clearance of 1 mm to 2 mm is enough, depending on the case toleranzes.

4. Optimization of Substrate Size

Applying the numbers found above, optimal substrate sizes can be found.
The final choice should consider the availabe standard sizes of the ceramic material. These are given in simple parts (1/4",1/2")and multiples of 1 inch(1 1/2",2",4",6")
For mechanical reasons and yield problems sizes exceeding 2" x 2" are not recommended.

4.1 Substrates with uncased chips

chip size	3 mm x 3 mm
chip spacings (high density)	2 mm to 3 mm
chips per substrate unit	$16/inch^2$
substrate complexity	32, 64,(96, 128 chips)

Optimal Substrate sizes with bare chips

	size	chips
chips at 1 side	1"x2"	32
	2"x2"	64
chips at 2 sides	1"x1"	32
	1"x2"	64
	(2"x2"	128)

4.2 Substrates with flatpacks T091

Only the double side technique is considered because of its well proven reliability and its need of only 50 % in volume and weight as compared with the single side technique.

Optimal substrate sizes with flatpacks T091

	size	flatpacks
Flatpacks at both sides	1"x1 1/2"	16 [1]
	1"x2"	24 [2]
	1 1/2"x2 [3]	32
	2"x2"	48 [2]

1) Unsufficient complexity
2) Unsuitable circuit partition
3) No standard substrate

D) SUBSTRATE INTERCONNECTION SYSTEMS

Flexible PCBs for Substrate Interconnection

Thin flexible printed circuit boards would be the conventional technique to interconnect all the leads on 1, 2, 3, or 4 sides of the stacked substrates.

For the present application some disadvantages have to be considered:

1) The use of the memory unit in space projects would be restricted since, generally speaking, plastic (organic) materials are not permitted.

2) For each space application the following disadvantages have to be checked:

   2.1 Outgassing (not only under vacuum; aggressive hardener and softener vapours may affect chips under normal pressure too).

   2.2 The leakage currents caused by radiation ionized plastics may become a problem with very high resistive circuits (MOS, CMOS).

3) The leakage currents, caused by the absorbed water molecules and hardener ions may become a problem with very high resistive circuits (MOS, CMOS).

4) Because of the water absorbing chemistry of all organic materials, warping of the PCB by drying or wetting during changes of humidity and/or atmospheric pressure may cause mechanical stress. This can result in fractures and openings of the copper circuit paths and solder connections.

5) The same failures may occur during changes of temperature (soldering, temperature cycling and shocks) because of warping caused by the thermal mismatch of the copper clad and the plastic laminate, and the ceramic substrate.

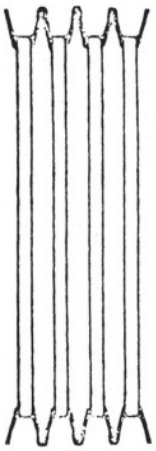
6) The flexible PCBs do not allow optical inspection of the substrates and solder connections behind them.

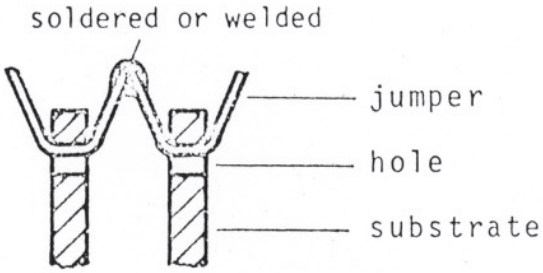
7) The flexible PCBs make the exchange of individual substrates (repair, inspection) difficult.
All the substrates have to be desoldered before disassembly. This repeated de- and resoldering of all substrates also decreases the unit's reliability.
All new solder interconnections must be checked and requalified.

8) The PCB interconnection system needs the highest number of solder joints. This decreases reliability.

To avoid these disadvantages, some PCB-free interconnection systems are proposed which have already been successfully delivered for space applications (e.g. ESTEC / Leitz/Lewicki sun sensor and ESTEC / Dornier/Lewicki power supplies).

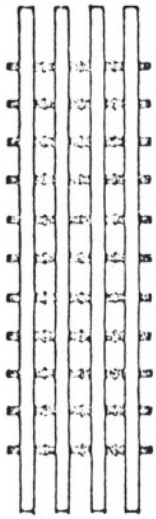
Here only unorganic materials are used (metals, ceramic) which do not change under vacuum, radiation, humidity or temperature influences. Also they allow free inspection of all substrates or packages and, some of them also allow the replacement of individual substrates without touching the others.
The number of solder joints is only 33 % to 50 % as compared with PCBs.

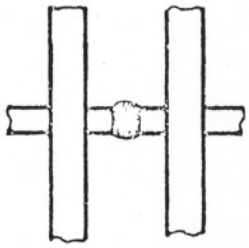




V-JUMPERs

view of the substrate edges, 1st plane (solder on substrate not shown)



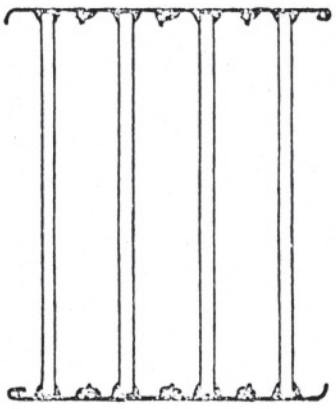


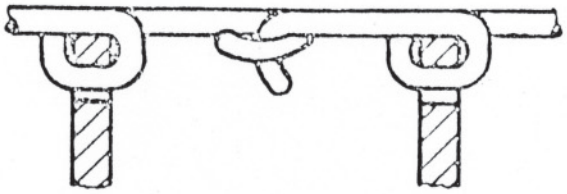
view of the substrate edges, 2nd plane

Multi-Substrate Packaging System
MSPS 7310 7310-01 "V-JUMPER"
INTERCONNECTION SYSTEM

LEWICKI micro-electronic

M

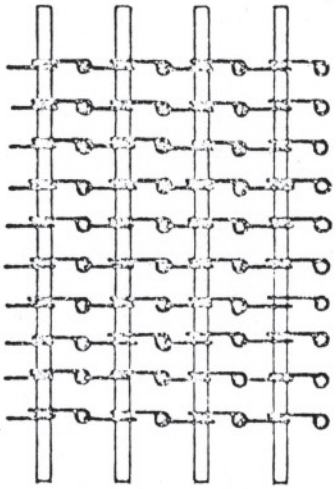




HOOK + EYE

view of the substrate edges , 1st. plane

(solder on substrates not shown)



HOOK + EYE

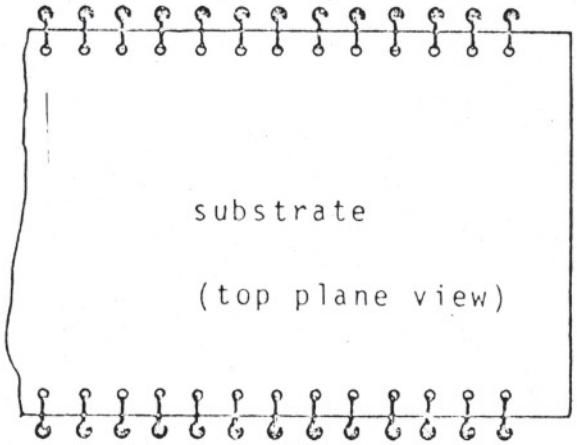
view of the substrate edges, 2nd. plane

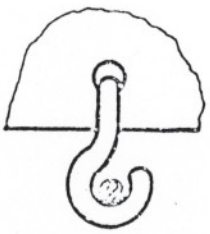
Multi-Substrate Packaging System
MSPS 7310

7310-02 "HOOK + EYE"
INTERCONNECTION SYSTEM

LEWICKI
micro-
electronic

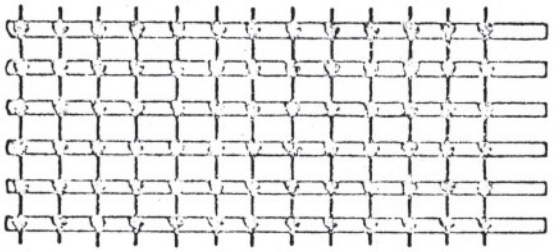
M





HOOK + BUS

(solder on substrate not shown)



substrate package
view of the edges

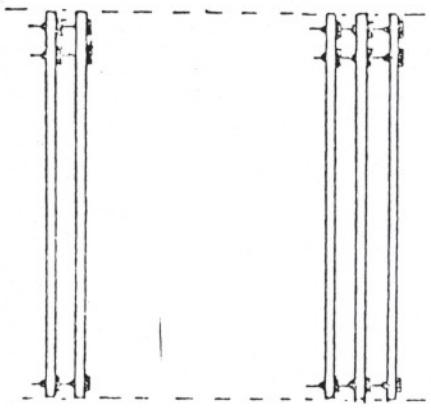
all rights reserved

Multi-Substrate Packaging System
MSPS 7310

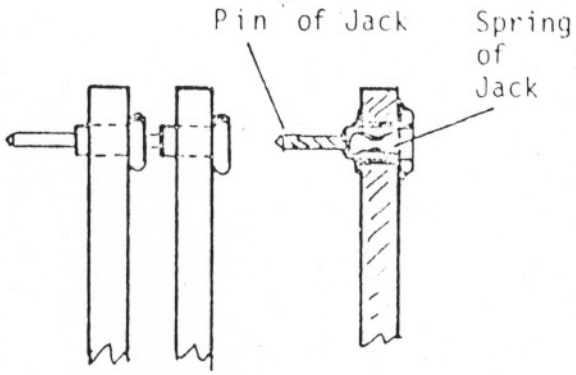
7310-03 "HOOK + BUS"
INTERCONNECTION SYSTEM

LEWICKI micro-electronic

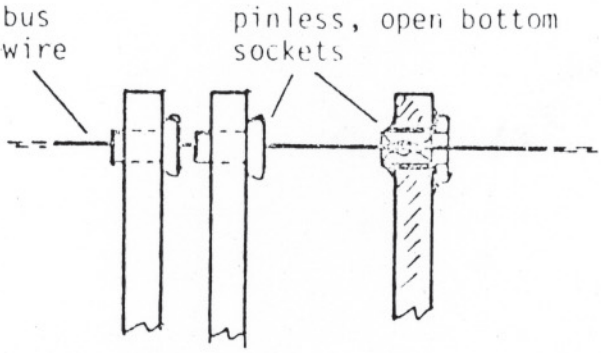
M



view of the substrate edges, 2nd plane



PIN-JACK Interconnection



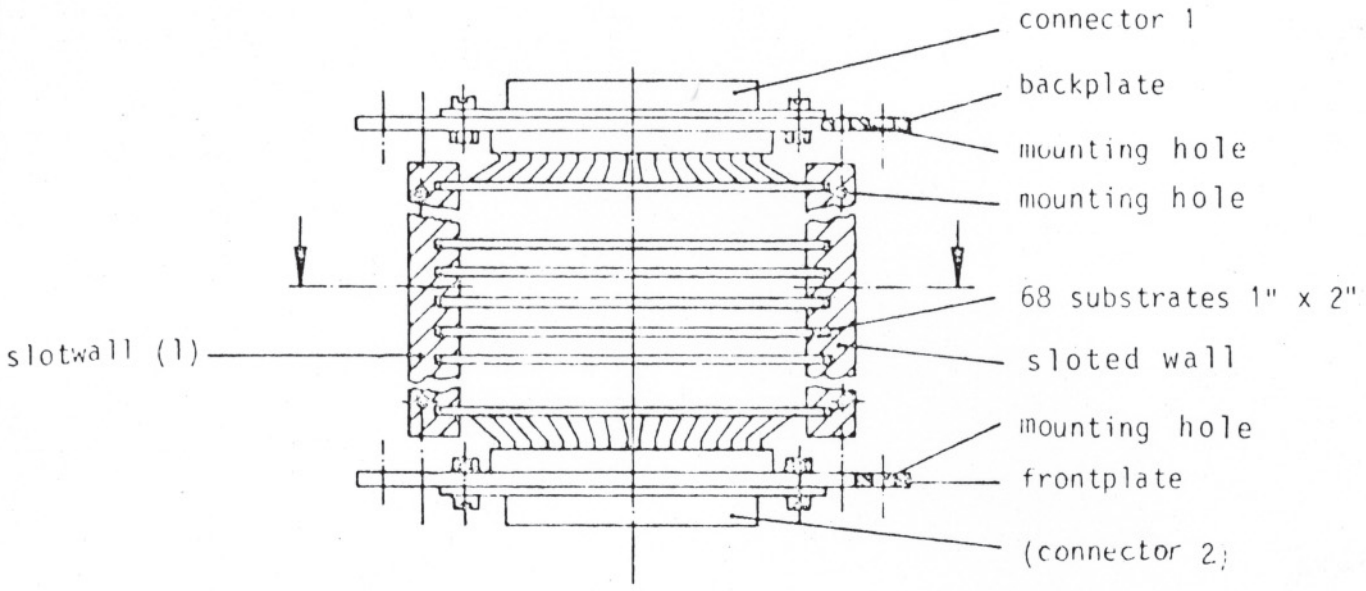
JACK + BUS Interconnection

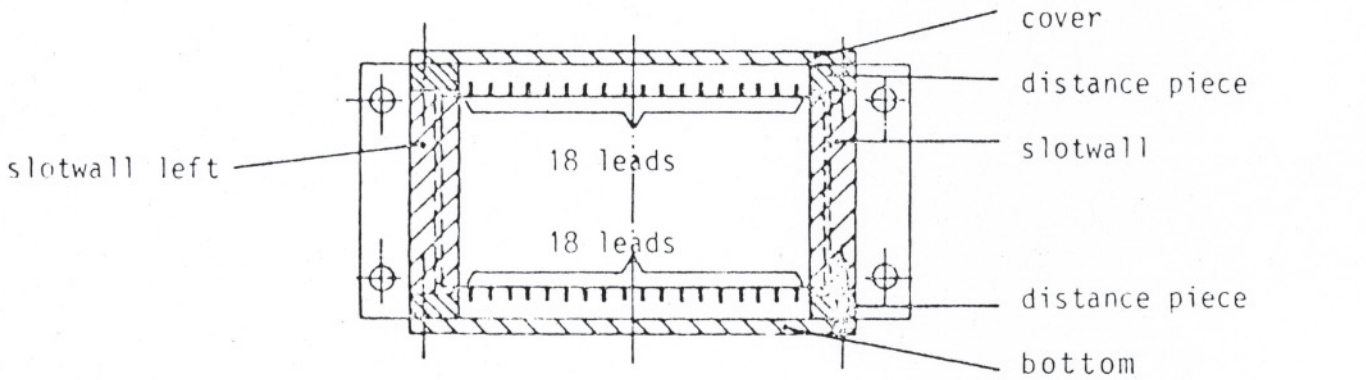
all rights reserved

Multi-Substrate Packaging System
MSPS 7310 7310-04 "PIN-JACK" INTERCONN.SYST
7310-05 "JACK + BUS"

LEWICKI micro-electronic

M





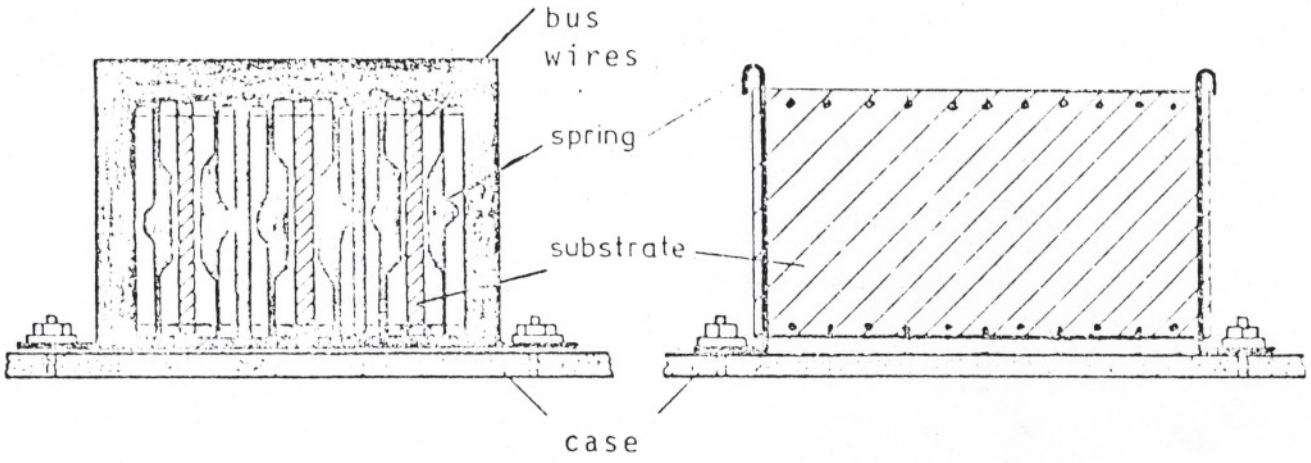
Cross section A-B

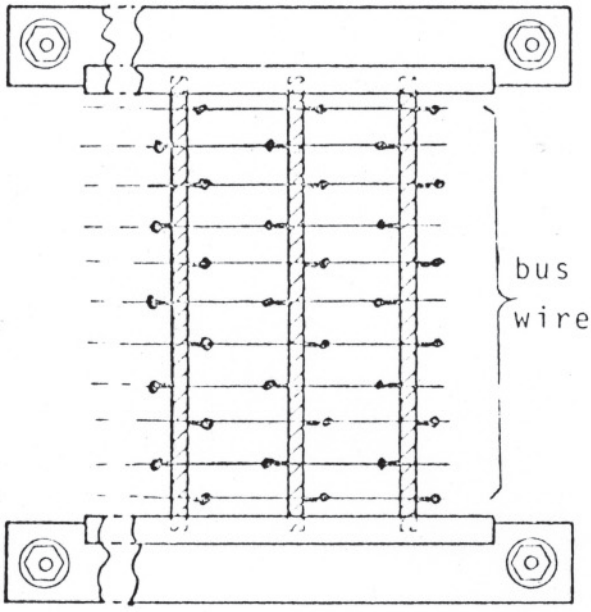
all rights reserved

Multi-Substrate Packaging System MSPS 7310		
LEWICKI micro-electronic		M

6.2 Light-Weight substrate Support System

A light-weight support system for multisubstrate mounting consists of 2 etched metal sheet-springs as shown below:

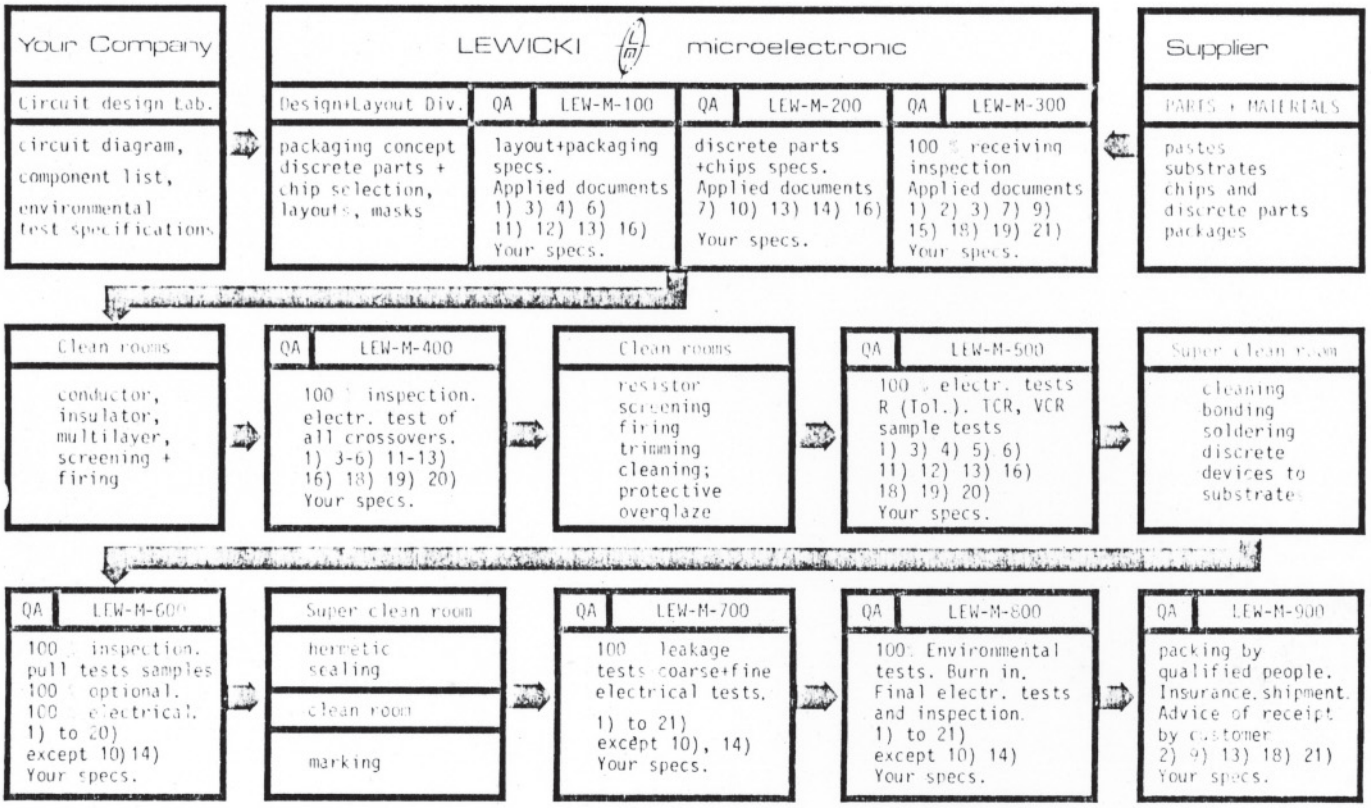




LIGHT WEIGHT MULTI SUBSTRATE SUPPORT SYSTEM

This support system allows the circuits to be removed without removing of the support system or other circuits. Furthermore, the support is elastic, by using springs so that the substrates will not brake by mechanical shock or thermal expansion.
It has been successfully used by the author for several Space projects, also for ESTEC (e.g LEITZ - LEWICKI Sun Sensor, DORNIER - LEWICKI Power Supplies).

E) QUALITY ASSURANCE FLOW PLAN



SPECIFICATIONS APPLIED

1.	MIL-M-38510	Microcircuits, general specification
2.	MIL-M-55565	Microcircuits, packaging
3.	MIL-STD-883	Test methods for microelectronics
4.	MIL-STD-1331	Parameters controlled for HICs
5.	NASA/85Mo3559	Line certification for HICs
6.	NASA/85Mo3926	Design and quality standards for custom HICs
7.	NASA/85Mo3927	Discrete chip devices for HICs
8.	NASA/ 1588	Soldering for highest requirements
9.	NASA/85Mo3916	Packaging, packaging and shipping
10.	NASA/ PPL	Prefered parts list
11.	NASA/ SP 508	The preventation of electrical breakdown in spacecraft
12.	ESRO/ QRC 02	Requirements for microwave ICs
13.	ESRO/ QRC 06	Procurement of qualified HICs
14.	ESRO/ QRC 31	Qualification of thickfilm HICs
15.	SCCC- PL	European electronic components and parts for space application
16.	GfW - 1000	IC group specification specs.
17.	GfW - IH-100	HICs procurement specifications
18.	GfW - 005	Zuverlässige Handlötungen / reliable handsoldering
19.	GfW - 006	Inspection system provisions for suppliers of space materials, parts, components and services.Product integrity procedure.
20.	GfW - AO-200 400,500	Inspection and control (900 radiografy)
21.	GfW - AO-300	Procedure for qualification
22.	GfW - AO-600	Packaging, marking, storage
23.	ASTM / ACMA	Specs and test methods for ceramic substrates

F) GENERAL HYBRID FABRICATION PLAN AND QA-ORGANISATION

GENERAL THICKFILM FABRICATION PROCESS
and
QUALITY ASSURANCE ORGANISATION PLAN
(not yet specially adapted to high density semiconductor memory multichip MSI/LSI microcirouits)

Material Tests (Q)
before production start

Substrates
pastes
(conductive,
dielectric,
resistive ,
protective)

fluxes

removers

Au + Al wires

Solders

packages
(lids, cover.
case, leads,
hermeticity)
solder preforms

gases

discrete devices
for incorporation
(Rs,Cs, Ls, diodes
Transistors, ICs)

Equipment Tests (Q) (calibration)
after programming
setting and adjusting

thickfilm printers

conveyor furnaces
trimming equipment

crossover + plate-
thru automatic testers

automatic dataprinters

bonders (die, chip, wire)
flipchip, beam lead

solder equipment
(dipping, reflow etc.)

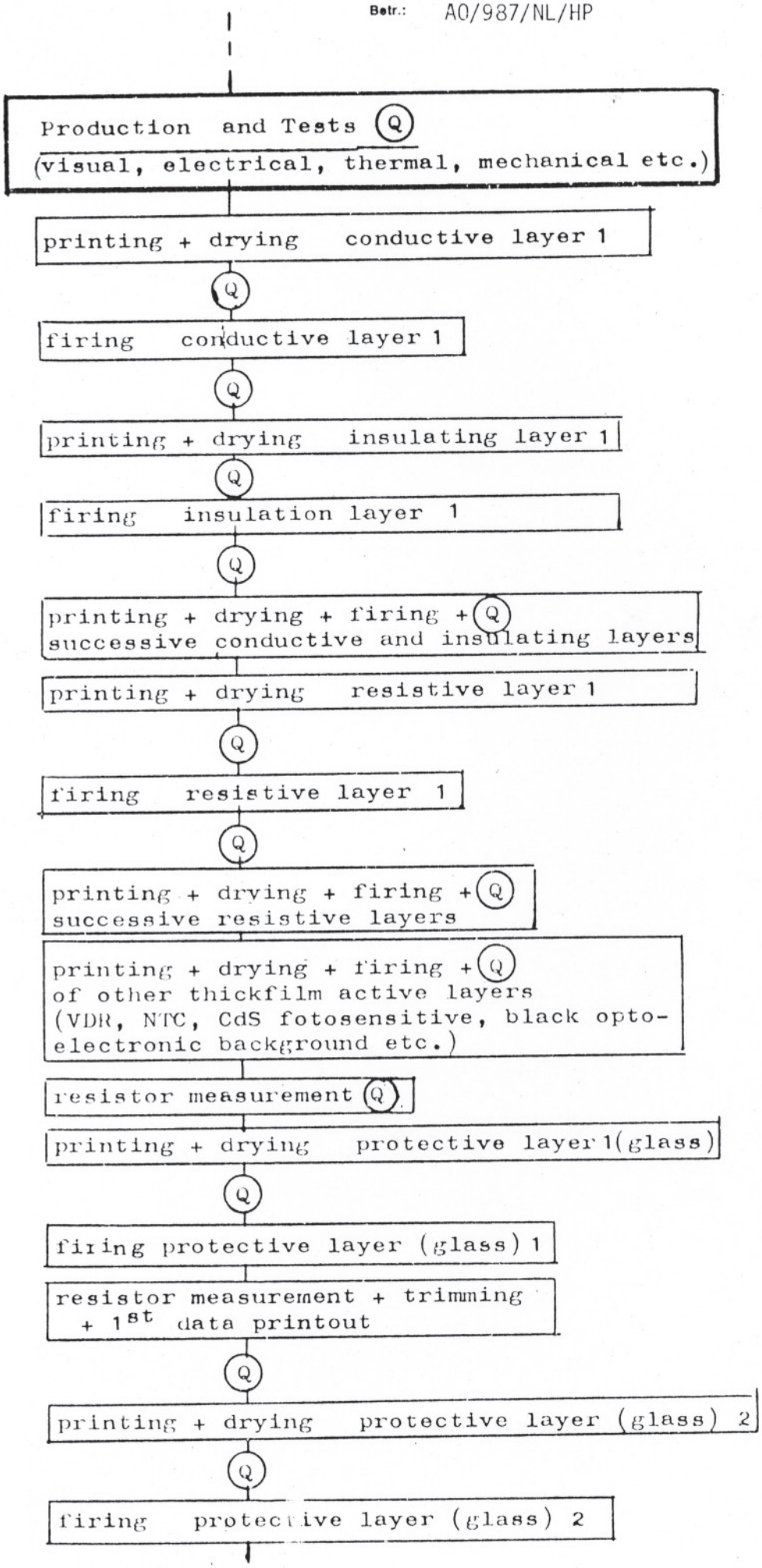
visual test equipment
(comparators)

leakage tester
(He detector)

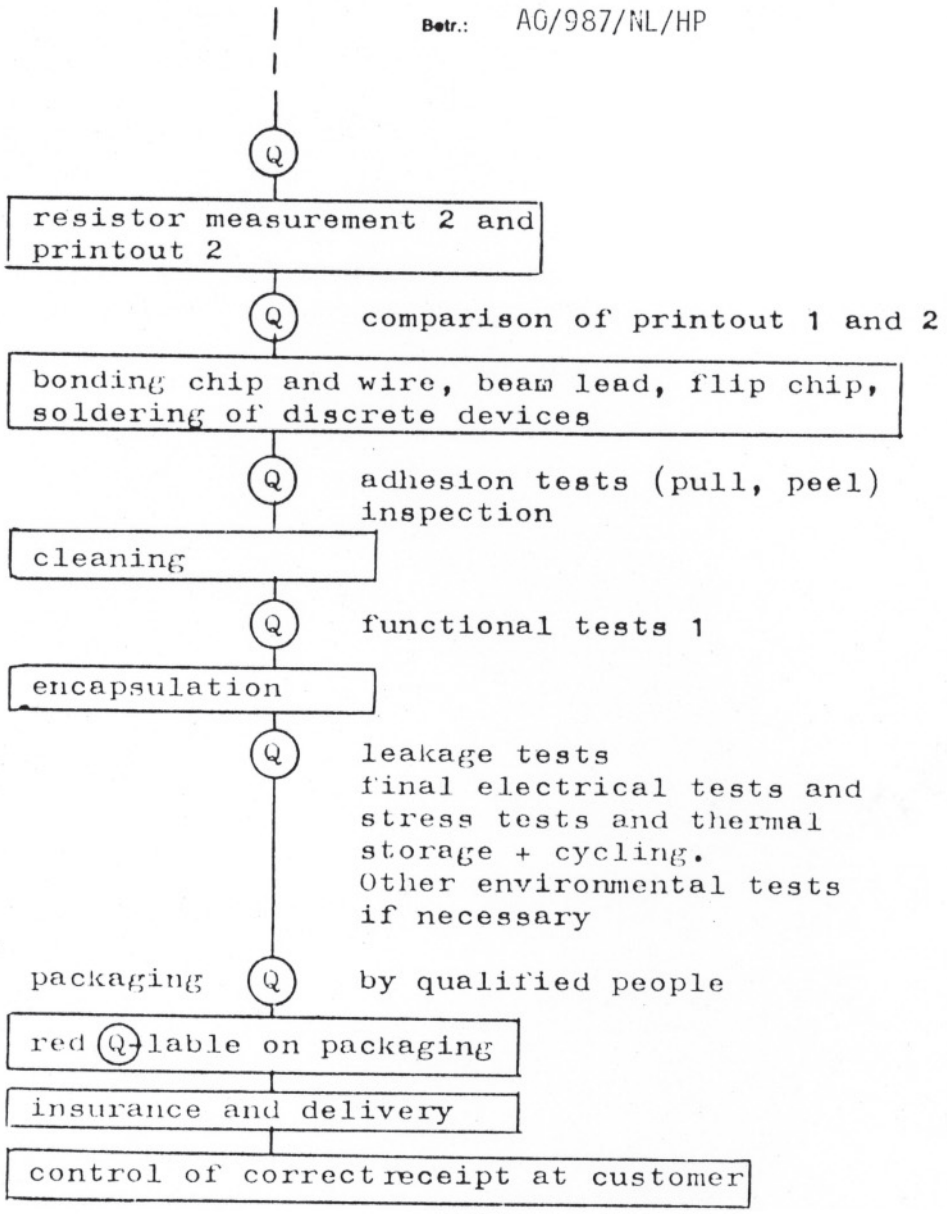
component part and IC
test equipment

functional hybrid IC
final test equipment

environmental test
equipment

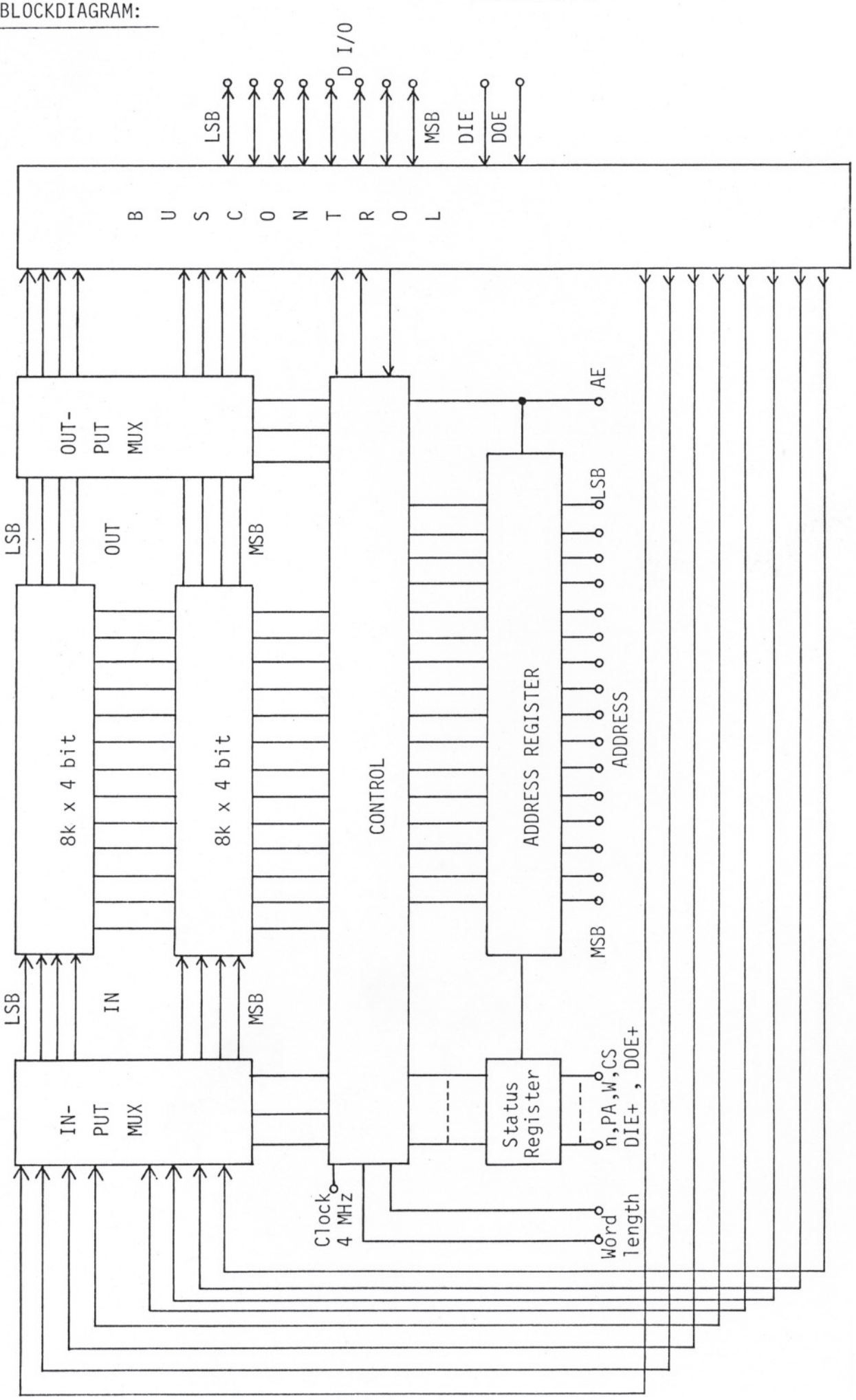


Für diese Unterlage behalten wir uns alle Rechte vor, auch für den Fall der Patenterteilung oder Gebrauchsmustereintragung. Ohne unsere vorherige Zustimmung darf die Unterlage weder vervielfältigt noch Dritt[illegible] zugänglich gemacht werden, und sie darf durch den Empfänger oder Dritte auch nicht in anderer Weise mißbräuchlich verwertet werden. Zuwiderhandlungen verpflichten zu Schadenersatz und können strafrechtliche Folgen haben.

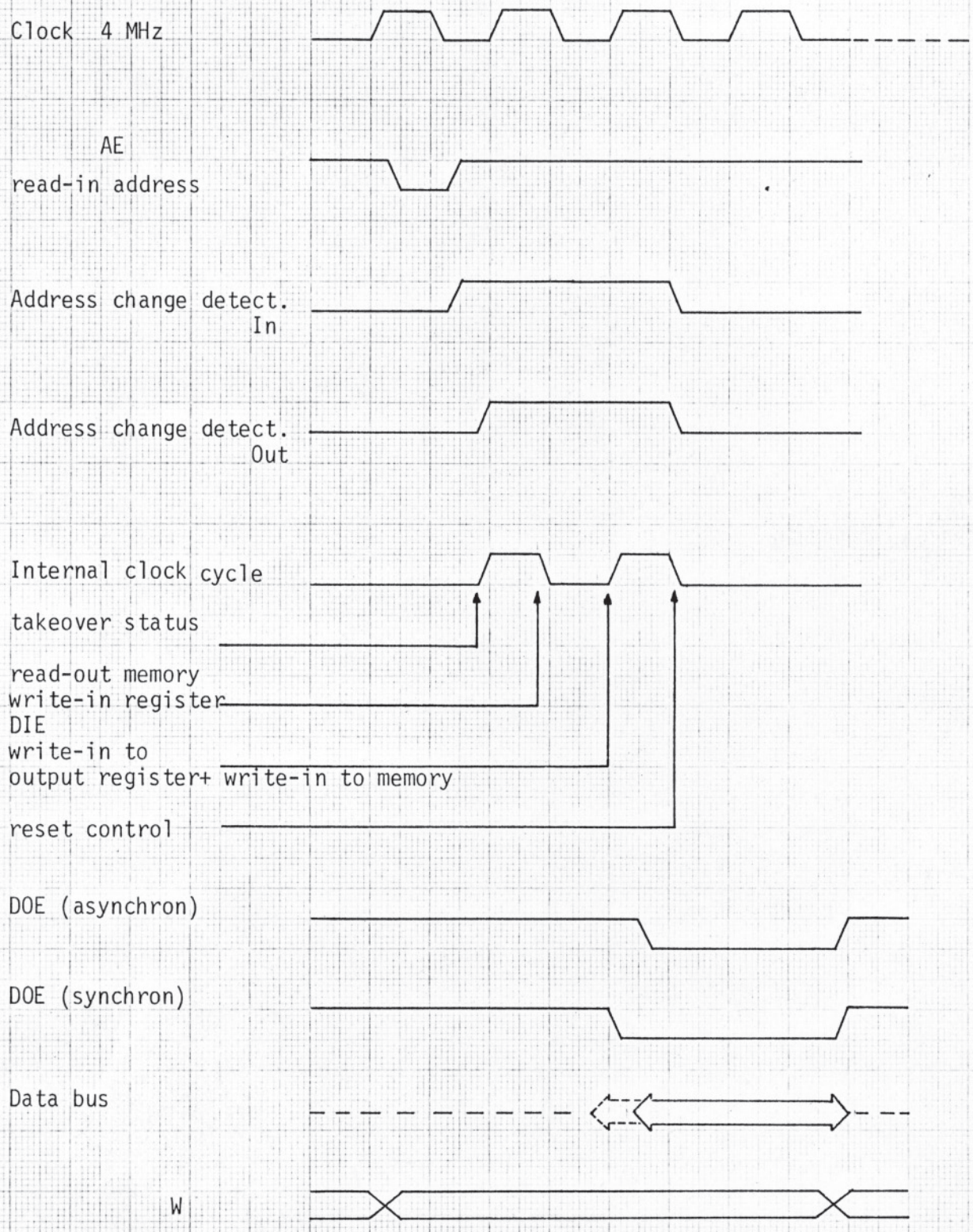


Für diese Unterlage behalten wir uns alle Rechte vor, auch für den Fall der Patenterteilung oder Gebrauchsmustereintragung. Ohne unsere vorherige Zustimmung darf diese Unterlage weder vervielfältigt noch Dritten zugänglich gemacht werden, und sie darf durch den Empfänger oder Dritte auch nicht in anderer Weise mißbräuchlich verwertet werden. Zuwiderhandlungen verpflichten zu Schadenersatz und können strafrechtliche Folgen haben.

To 1.2 BLOCKDIAGRAM:



To 1.2 P U L S E D I A G R A M :



1.2 Functional Description of the proposed CMOS Memories

Memory Organization

The memory system shall be built with 256 x 4 bit memory chips. It consists of 2 blocks of 8k x 4bit each. The 2 blocks will be parallel controled to give 8k x 8bit memory capacity.
The other word length of 16k x 4bit and 64k x 1bit will be made by multiplexing the 8bit in- and outputs of the memory blocks.

Address

The address to read or write a word, will be latched in an address register until a new address occurs.
Depending of the organization, several address word length will be decoded (counted from MSB) e.g. 13bit address for 8k x 8bit organization and 16bit address for 64k x 1bit organization.
The status of not used address bits can be arbitrary. After a new address is latched in the register, the memory control will be started to read or write data.

Data bus

The data bus has several word length depending on the used organization. The maximum word length will be 8 bit, the minimum word length will be 1 bit. Not used bits will have high impedance, because of tristate logic. The data bus will be bidirectional, so it can be used for input and output data. The number of used bits will be counted from LSB.
To read out data, the data bus will be activated by the DOE signal and the latched data will be put on the data bus.

Control

The control logic coordinates data input or output and the necessary internal operations like address setting, generation of the read/write signal and latchstrobe. Also an internal 4 MHz clock will be generated. For synchronous operations a external clock can be used.
A complete read or write cycle time consists of 2 clock cycles and will be less than 500 ns.
Another possibility to make the internal control instead derived from a clock, is by the use of gate transition times. This concept would give shorter cycle time, but it is not recommended because of temperature drift and degradation of these parameters.

Paging

The paging signal allows to divide the mainframe memory into blocks of a certain length.
For paging the most significant bits will be decoded for a block-address, the least significant bits are the address in the block.
It is assumed that the max. number of blocks will be 8 (2^3).
To set the block number desired, the exponent n (n=0...3) will be latched in the status register synchronous to the address.
The n-signal only changes the block length when the paging signal is set.

Status

The signals : n = exponent of the block numbers
W = read / write signal
DIE^+ = data-in enable, for synchronous operation
DOE^+ = data-out enable, for synchronous operation
CS = memory select
and PA = paging ,
will be latched in the status register synchronous to the address for one read or write cycle.
The signals DIE^+ and DOE^+ are for address synchronous operations.
In this case DIE and DOE must be set to the high level.
For asynchronous operations, DIE^+ and DOE^+ must be set to high level and the memory access can be done by DIE and DOE.

Memory expansion to 144k

To get the 144k memory, three of the before described 64k memories shall be connected parallel.
For example: The 144k memory organized to 8k x 18 bit consists of two modules organized to 8k x 8 bit and one module organized to 32k x 2 bit (24k not used).

The 144k memory organized to 16k x 9 bits consists of two modules organized to 16k x 4 bit and one module organized to 16k x 1 bit (48k not used).

Power consumption

Due to the high speed operation a supply voltage $V_{DD} \approx 15$ V will be used.
The quiescent supply current will be less than 50 mA for a modul.

Parts

The memory will be built up with qualified radiation hardenend parts.

1.3 Description of the technical options

On the basis of 256x4 bit memory chips the technical options of development for the 64kbit or 144kbit memories are given below:

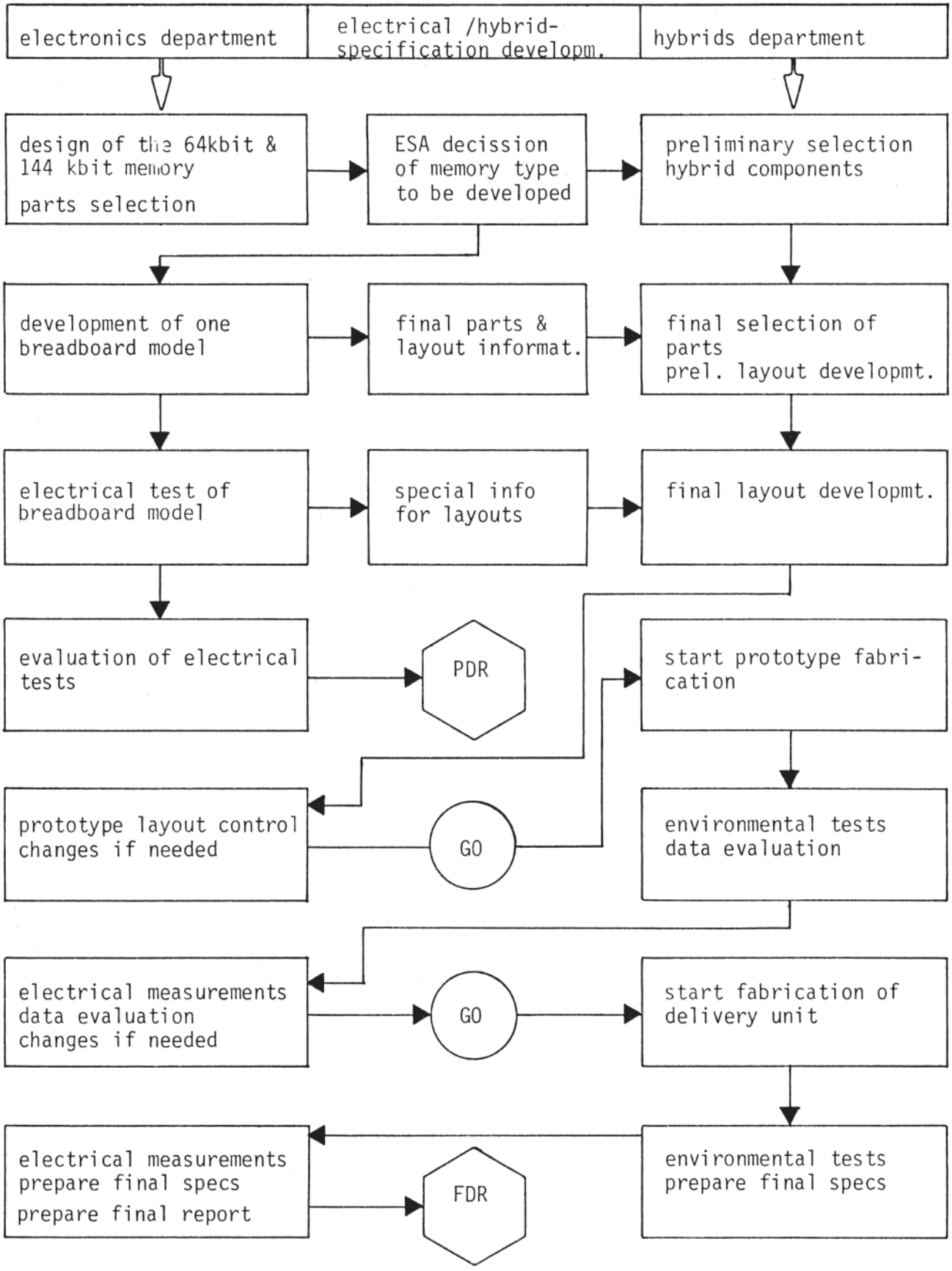
64kbit-memory	concept AC-1	concept AC-2	concept CC
Volume:	2 substrates	4 substrates	6 substrates
Weight:	8 Gramm	16 Gramm	60 Gramm
Substrate Size:	1" x 2"	1" x 2"	1" x 2"
Chips/Substrate:	64	32	20-24
Chip Protection:	none or resin drop/none or resin drop/flatpacks		
Power:Steady state power consumption appr. 500 mW.			

This description shows the advantage of the concept AC-1 with only two substrates needed. In accordance with the QRC-06 (oct.74) and QRC-31 (dec.74) the use of non-prepackaged semiconductor chips in HMs is allowed, so the AC-1 concept should be used for the proposed development.
One substrate includes the complete memory chips and the other one includes the memory logic.

144kbit-memory	concept AC-1	concept AC-2	concept CC
Volume:	4 substrates	8 substrates	12 substrates
Weight:	16 Gramm	32 Gramm	120 Gramm
Substrate Size:	1" x 2"	1" x 2"	1" x 2"
Chips/Substrate	64	32	20-24
Chip Protection:	none or resin drop/none or resin drop/flatpacks		
Power:Steady state power consumption appr. 1000mW.			

Also here the concept AC-1 shows the same advantage. Alternatives to the above options are substrates with 2" x 2" size. The 64kbit memory could be developed on a single substrate and the 144kbit memory would need only two substrates of this size. Final decisions should be made when the packaging system of the s/c electronics are known.

2. FLOW CHART OF THE PROGRAM



3. # WORK PACKAGE DESCRIPTION

PC 20/1

PROJECT AO/987/NL/HP (64/144kbit memory) PHASE :	W.P. REF. :
W.P. TITLE Overall workpackage CONTRACTOR MAJOR CONSTITUENT (e.g. Subsystem) START EVENT 1 PLANNED DATE TBD END EVENT 56 PLANNED DATE TBD W.P. MANAGER	SHEET 1 OF 14 ISSUE REF. ISSUE DATE

General Information:

The following work package (WP) descriptions (page 2 to page 14) show the development and fabrication process within normal working hours.
If the project desires shorter delivery times, parallel work and overtime work are neccessary to decrease schedule duration.

WORK PACKAGE DESCRIPTION

PC 20/1

PROJECT	AO/987/NL/HP		PHASE :		W.P. REF :
W.P. TITLE	Design 64/144kbit CMOS Memory				SHEET 2 OF 14
CONTRACTOR					
MAJOR CONSTITUENT (e.g. Subsystem)					ISSUE REF.
START EVENT	week 1	PLANNED DATE	TBD		ISSUE DATE
END EVENT	week 10	PLANNED DATE	TBD		
W.P. MANAGER					

1. receive spec's from electronics department
2. design software package of 64kbit and 144kbit CMOS memory
3. prepare documentation for ESTEC review
4. receive ESTEC decission of memory type to be developed
5. prepare parts list for hybrid department

WORK PACKAGE DESCRIPTION

PROJECT	AO/987/NL/HP	PHASE :		W.P. REF :
W.P. TITLE	Pre-Selection of Hybrid Components			SHEET 3 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 9	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 12	PLANNED DATE	TBD	
W.P. MANAGER				

1. receive preliminary parts list from electronics department
2. select parts from prefered parts list, check second source
3. check delivery times
4. prepare complete preliminary parts list for final selection

WORK PACKAGE DESCRIPTION

PC 20/1

PROJECT	AO/987/NL/HP		PHASE :		W.P. REF :
W.P. TITLE	Breadboard Development 64 or 144kbit-mem.				SHEET 4 OF 14
CONTRACTOR					
MAJOR CONSTITUENT (e.g. Subsystem)					ISSUE REF.
START EVENT	week 11	PLANNED DATE	TBD		ISSUE DATE
END EVENT	week 15	PLANNED DATE	TBD		
W.P. MANAGER					

1. receive documentation (schematics, blockdiagrams etc.)
2. order of-the-shelf standard CMOS, Cs etc.
3. develop b.b. hardware with EURO-card pcb's and wire-wrap system
4. built b.b.-test-equipment on wire-wrap pcb's in standard electronic box
5. give final parts and layout information to hybrid department
6. prepare b.b. for electrical tests

WORK PACKAGE DESCRIPTION

FC 20/1

PROJECT	AO/987/NL/HP		PHASE :	W.P. REF :	
W.P. TITLE	Electrical Test of Bread-Board Model			SHEET 5 OF 14	
CONTRACTOR					
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.	
START EVENT	week 16	PLANNED DATE	TBD	ISSUE DATE	
END EVENT	week 18	PLANNED DATE	TBD		
W.P. MANAGER					

1. prepare test plan and procedure
2. electrical measurements:
   a. functional tests with various test patterns (ESSTEC approved), tested special test equipment
   b. test of power consumption with variable transfer frequencies
   c. temperature test
3. verify electrical specifications as per ESTEC THH/553/PM/WW/CV paragraph 3.6
4. give special information to hybrid department for final layout development (e.g. shieldings on signal lines etc.)
5. set date for PDR and mid-term presentation with ESTEC

WORK PACKAGE DESCRIPTION

PC 20/1

PROJECT	AO/987/NL/HP		PHASE :	W.P. REF :
W.P. TITLE	Evaluation of Electrical Tests			SHEET 6 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 19	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 19	PLANNED DATE	TBD	
W.P. MANAGER				

1. receive test reports
2. internal review of test results
3. prepare list of deviations
4. prepare documentation of PDR
5. send PDR documentation to ESTEC
6. receive "GO" for fabrication of prototype unit

WORK PACKAGE DESCRIPTION

PC 20/1

PROJECT	AO/987/NL/HP	PHASE :		W.P. REF :
W.P. TITLE	Final Parts Selection and Pre-Layout			SHEET 7 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 13/19	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 20/25	PLANNED DATE	TBD	
W.P. MANAGER				

1. receive final parts and layout information from breadboard model
2. select final parts from PPL
3. order needed parts and materials (incl. spares)
4. start layout development
5. check preliminary layout

WORK PACKAGE DESCRIPTION

PROJECT	AO/987/NL/HP	PHASE :		W.P. REF :
W.P. TITLE	Final Layout Development			SHEET 8 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 26	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 28	PLANNED DATE	TBD	
W.P. MANAGER				

1. receive preliminary layout
2. develop final layout
3. check final layout with electronics department
4. include changes, if necessary
5. prepare documentation for prototype fabrication
6. receive "GO" for prototype fabrication

WORK PACKAGE DESCRIPTION

PC 20/1

PROJECT	AO/987/NL/HP	PHASE :		W.P. REF :
W.P. TITLE	Prototype Fabrication			SHEET 9 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 28	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 44	PLANNED DATE	TBD	
W.P. MANAGER				

1. produce fotomasters and masks
2. start fabrication according to process described on page 21

WORK PACKAGE DESCRIPTION

PROJECT	AO/987/NL/HP		PHASE :	W.P. REF :
W.P. TITLE	Electrical Tests of Hybrid Prototype			SHEET 10 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 29	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 46	PLANNED DATE	TBD	
W.P. MANAGER				

1. electrical tests during fabrication according to fabrication plan (page 21)
2. final electrical measurements
3. data evaluation
4. document changes, if needed
5. give final "GO" to hybrid department for fabrication of delivery unit

WORK PACKAGE DESCRIPTION

PROJECT	AO/987/NL/HP		PHASE :	W.P. REF :
W.P. TITLE	Environmental- and Material Tests Prototype			SHEET 11 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 29	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 47	PLANNED DATE	TBD	
W.P. MANAGER				

1. environmental and material tests according to fabrication plan
2. final environmental tests
3. data evaluation

WORK PACKAGE DESCRIPTION

PROJECT	AO/987/NL/HP	PHASE :		W.P. REF :
W.P. TITLE	Fabrication of Delivery Unit			SHEET 12 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 49	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 52	PLANNED DATE	TBD	
W.P. MANAGER				

1. incorporate changes if necessary
2. fabricate according to fabrication plan

WORK PACKAGE DESCRIPTION

PROJECT	AO/987/NL/HP		PHASE :		W.P. REF :
W.P. TITLE	Electrical Tests of Delivery Unit				SHEET 13 OF 14
CONTRACTOR					
MAJOR CONSTITUENT (e.g. Subsystem)					ISSUE REF.
START EVENT	week 49	PLANNED DATE	TBD		ISSUE DATE
END EVENT	week 54	PLANNED DATE	TBD		
W.P. MANAGER					

1. electrical tests during fabrication according to fabrication plan
2. final electrical measurements
3. data evaluation
4. prepare final electrical specifications
5. prepare electrical part of final report
6. prepare documentation for FDR and final presentation
7. send FDR documentation to ESTEC

WORK PACKAGE DESCRIPTION

PROJECT	AO/987/NL/HP		PHASE :	W.P. REF :
W.P. TITLE	Environmental Tests of Delivery Unit			SHEET 14 OF 14
CONTRACTOR				
MAJOR CONSTITUENT (e.g. Subsystem)				ISSUE REF.
START EVENT	week 49	PLANNED DATE	TBD	ISSUE DATE
END EVENT	week 56	PLANNED DATE	TBD	
W.P. MANAGER				

1. environmental and material tests according to fabrication plan
2. final environmental tests
3. data evaluation
4. prepare final specifications
5. prepare environmental part of final report
6. prepare documentation for FDR and final presentation

4. Cost Plans

4.1 Cost plan of the 64kbit Memory Option

PC 36.4
Sheet 1 of 2

Subject: 64kbit - CMOS Memory

PRICE BREAKDOWN FORM

Ref.: AO/987/NL/HP

Local Currency: DM

Tenderer / proposed sub-contractor:

Date of Issue: 20.7.78

1 LABOUR COST

Category	Total Manpower Effort in Manhours	Basic Hourly Labour Rate	Labour Overhead %	Labour Overhead Rate	Gross Hourly Labour Rate	Total Cost Local Currency	Total Cost AU
A	1.875	29,64	30	8,88	38,52	72.225,--	
B	1.650	19,80	30	5,94	25,74	42.471,--	
			Total Labour Cost			114.696,--	

2. MATERIAL COST

Category	Direct Cost	Material Overhead (if applicable) %	Material Overhead (if applicable) Amount	
parts & materials	9.400,--	20	1.880,--	11.280,--
test equipment	8.400,--	20	1.680,--	10.080,--
		Total Material Cost		21.360,--

3 INTERNAL SPECIAL FACILITIES (if applicable)

Category	Hours of Use	Hourly Rate		
not applicable				
		Total Cost of Internal Special Facilities		

4 GENERAL & ADMINISTRATIVE OVERHEAD AND GENERAL RESEARCH & DEVELOPMENT CONTRIBUTION (if applicable)

	%	Total Amount of 1 and/or 2 and/or 3		
General & Administrative Overhead				
General Research & Development Contribution	5	136.056,-	6.802,80	
		Total G & A Overhead and General R & D Contribution	6.802,80	

5. PRIME COST (1 + 2 + 3 + 4)

5.	PRIME COST (1 + 2 + 3 + 4) (carried forward)				142.858,80	
6.	OTHER DIRECT COST	Direct Cost	Overhead (if applicable)			
	Category		%	Amount		
	External Major Products					
	External Special Equipment					
	External Services					
	Travel and Subsistance	2.400,--	---	---	2.400,--	
	Packing and Shipping					
			Total Other Direct Cost		2.400,--	
7.	SUBTOTAL (5 + 6)					
8.	LICENCE FEES AND ROYALTIES					
	Description	Licensor	Basis of calculat.	Rate %		
	not applicable					
			Total Licence Fees and Royalties		-----	
9.	NOMINAL PROFIT		Amount of 5	Rate %		
			142.858,80	5	7.142,94	
10.	*ADDITIONAL PROFIT (IF APPLICABLE)		Amount of 5	Rate %		

11.	TOTAL PRICE (5 + 6 + 8 + 9 + 10)				152.401,74	

4.2

Additions for the 144kbit memory development and fabrication:

1. Labour Cost "A"	125 h = 3.705,--(+30%)= 1.111,50	4.816,50
" " "B"	85 h = 1.683,--(+30%)= 504,90	2.187,90
2. Material Cost	7.280,--(+20%)= 1.456,--	8.736,--
Total Additions		15.740,40
3. + 5% of pos. "4"		787,02
		16.527,42
4. + 5% of pos. "9"		826,37
Total price of 144kbit additions to the above price breakdown for the 64kbit memory.		17.353,79

* This item is not standardised and may be changed on a case by case basis

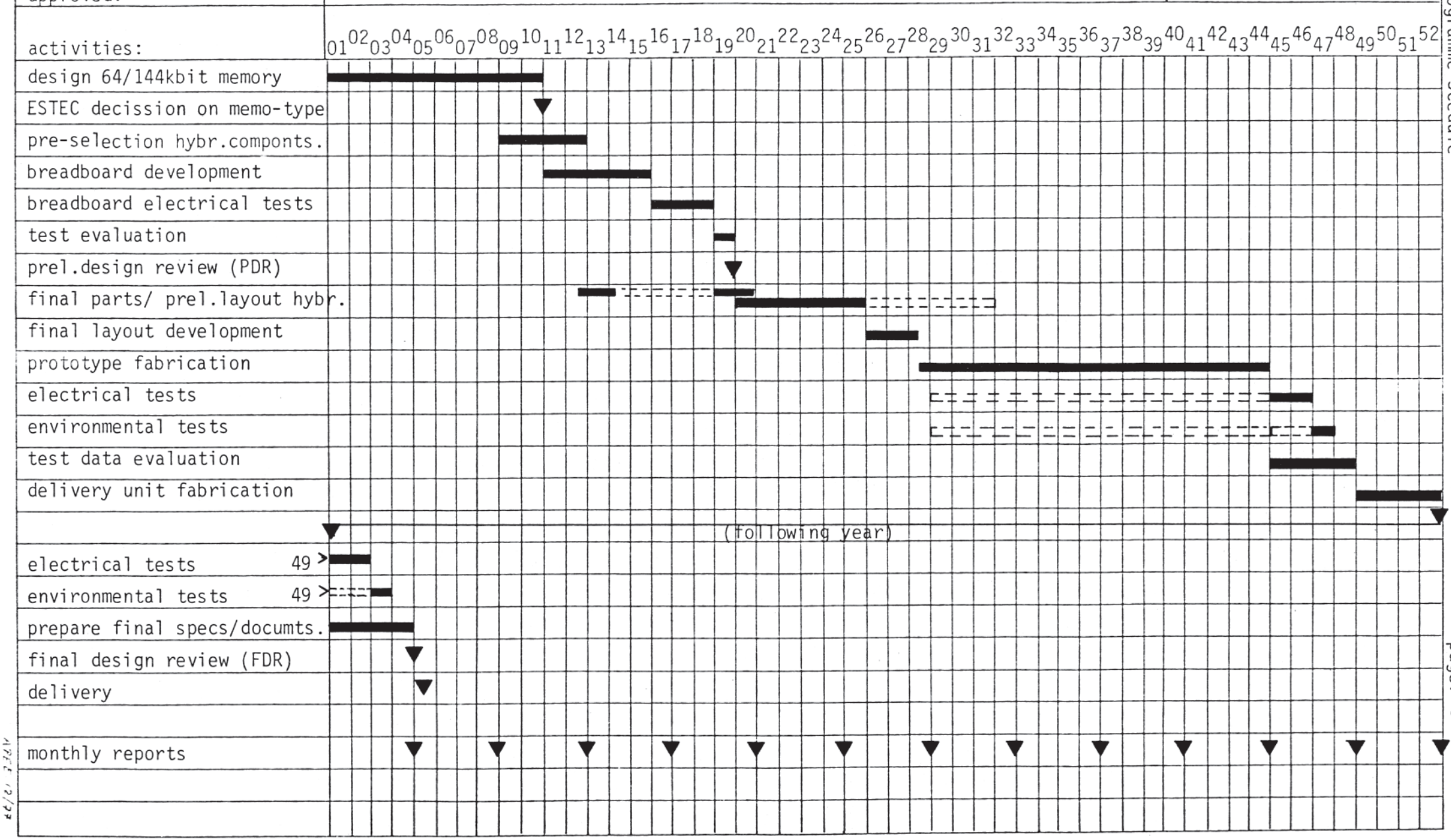
prepared:
approved:

MILESTONE-SCHEDULE of year: ..... of contract

project: ESTEC offer request no. AO/987/NL/HP

orig.-date: 19.7.1978
rev. -no. :
rev. -date:
page: ___ of:

5. Programme Scedule



6. K E Y - P E R S O N N E L

Dipl.-Ing. Andreas Lewicki

Studies "Nachrichtentechnik" from 1954 to 1959 at Technische Hochschule München, Diploma with a very-low-frequency-ton-generator in optoelectronics version, different positions at AEG -Telefunken research laboratories, 1965 management of space projects and microelectronics at AEG-Telefunken, since 1967 startet private hybrid laboratories and fabrication in Ulm, 1978 founded Lewicki Microelectronics,LTD, Tullamore, Ireland, more details see on page 54 "Lewicki Chronology".

Mr. A.Lewicki is prepared to spend 5% of his time to this project.

Dr.rer.nat. Johannes Huber

Studies "Electronics and Technical Physics" from 1963 to 1969 at Technische Hochschule, München.
1969 to 1974 at Physical Institute of University of Neuchatel,Switzerland, where he received his Dr. degree.
In 1975, scientific assistent at Bundeswehr Hochschule München, Institute for Flow Research.
Since 1976 at Lewicki Microelectronics as head of the department for the Fabrication of Analog and Digital Hi-Rel Hybrid IC's.
Experience in the cooperation with national and international Aeronautic and Space Industrie like MBB, Dornier, DFVLR, ESA and NASA.
Dr. Huber is prepared to spend 45% of his time to this project.

Dipl.phys. Donalt Bach

Physical studies from 1971 to 1978 in the field of Solid-State-Physics, Geophysics and LASER.
At Lewicki Microelectronics responsible for R&QA in the department for Analog and Digital Hi-Rel Circuits.
Experience in the cooperation with national and international Aeronautic and Space Industrie like MBB, Dornier, DFVLR, ESA and NASA.
Mr. Bach is prepared to spend 30% of his time to this project.

7. Facilities

With the exception of salt-spray tests, all required tests can be performed by the tender organisation.
A complete inventory list of the tenderers equipment in use was prepared by Mrs. Houlberg and Mr. Boetti of ESTEC and can be used for verification of compliance with the QRC-31/C.

In addition, Lewicki microelectronics Ltd. Ireland, founded in 1977 (2000 square meters plant, 100 hi-rel experienced final employment) offers:

Important additional environmental, electrical and optical test equipment (loose particle impact noise detector, vibration, shock, centrifuging 50.ooo g, computerized burn-in and crossover, thermal vacuum, thermal cycling, helium mass spectroscopy, viscosimeter) and production equipment (f.i. second electron beam welding machine for hermetic hybrid package sealing, Teradyn W311 computerized laser Resistor Trimmer).

8. Experience of the Tenderer Organisation and the Consultants

LEWICKI Chronology

1960 Optoelectronic function generator (pat.a.f.)

1962 Thinfilm Hybrid-IC and optoelectronic technology. Eutectic chip bonder. Evaporation mask system. Patents on light emitting diode (led) devices.

1965 Space projects and microelectronics management at AEG-TELEFUNKEN.

1966 Book publication: Lewicki "Introduction to Microelectronics", R.Oldenbourg Verlag, 588 pages.

1967 Award of the NTG/VDE (German Telecomm.Soc.) for the best electronics publication in 1966.

1967 Private Custom Hybrid-IC design laboratory and microelectronics consulting for aerospace industry and institutes.

1970 Over 100 different Hybrid-ICs designed and produced.

1972 New 1000 m^2 plant for hi-rel Hybrid-ICs built.

1976 Over 450 different hi-rel Hybrid-ICs designed and produced for importand space projects (e.g. HELIOS, AZUR, AEROS, GEOS) and for military (e.g. MRCA, LEOPARD), nuclear, medical and oceanological applications.

1977/78 Several proposals prepared for space experiments in future missions (e.g. GALILEO, OOE). Serial production of heart pacemakers according to the specifications of the FDA Medical Device Amendments which became US public law 94-295 in 1976.

1977 Lewicki microelectronics, LTD., Tullamore/Ireland, was founded. The factory has 2000 square meters in size and includes most modern equipment (e.g. 100.000g Triotec centrifuge). 100 experienced employes final capacity. (electron beam welder, Teradyn W311 Laser Trimmer)

Lewicki Microelectronics participated for example in the following ESA/ESTEC projects:

- contract no. ESTEC 2119/73 HP, "memoires autoreparables a semiconducteurs", study with Intertechnique/France.
- GEOS mass spectrometer and energyspectrometer S-303 of Uni Bern, Contraves, Dornier, MBB and Max-Planck-Institute für Physik und Astrophysik.
- Digital semiconductor sun sensor of control and stabilization devision ESTEC (Mr.Soderholm, Dr.David, Mr. Helmke and Mr. Mehwald) and optical sensor section ESTEC (Mr. Morgenstern)

Consultants of Arbeitsgemeinschaft zur Planung und Entwicklung von Elektroniksystem (Arge P.E.E.S.) are Mr. F.Eckl, Mr. P.Gammelin and Mr. D.Semder.

- experienced in military hi-rel equipment since 1958
- Co-experimenters, lead-, design- and test-engineers at NASA, scientific institutes, government organisations and space industry in projects HEOS/A2, AEROS, HELIOS, Pioneer Venus, GALILEO and O.O.E.
- Since 1977 private consulting engineers.

Hybrid-ICs for the HELIOS Sun Probe

A. Lewicki, Microelectronic,
Oberdischingen/BRD

Summary

More than 1000 thick film hybrid ICs and thick film ceramic parts (42 different types) were developed and produced for the largest German space-project, the German/American HELIOS sun probe by LEWICKI, MICROELECTRONIC. Almost half of the scientific measuring apparatus on board the spacecraft is equipped with them. These devices demonstrate mainly the extreme areas of application of the thick film technology: – high voltage cascades and resistor networks in the meg to gigohm range with high stability and precision for the generation, control and distribution from 1 kV up to 6 kV direct current; precision ceramic substrates for "Channeltron" semiconductor miniature secondary electron multipliers; new techniques for the precise mounting and positioning of ceramic substrates; special fluxfree soldering with lead and cadmiumfree special solders; compact, shock and vibration resistant complex ceramic Space-Packs® modules, incorporating ferrite core transducers and diodes for driving 3 HELIOS core memories; specially sawn, ground and drilled ceramic substrates functioning as non-degassing, inorganic, miniature high voltage printed circuit boards with plated troughholes; high voltage insulating and screening tubes; supporting substrates for miniature mercury capillary relays for 1 kV d. c.; miniature collector caps for "Channeltrons" and more.

All thick film components have successfully passed the HELIOS space environmental tests. These include vacuum, thermal cycling and thermal vacuum tests. In addition, the tests required by GfW and NASA specifications for humidity, shock and vibration as well as electrical stress testing in normal atmospheres have been passed.

In this year at Oberdischingen near Ulm a new factory of more than 1000 square metres will be completed for the development and production of hybrid circuits for the scientific, military and civil aerospace, atomic energy, oceanology and medicine.

NBST THE NATIONAL BOARD FOR SCIENCE AND TECHNOLOGY
AN BÓRD NÁISIÚNTA EOLAÍOCHTA AGUS TEICNEOLAÍOCHTA

Shelbourne House, Shelbourne Road, Dublin 4, Ireland Telephone: Dublin (01) ~~601486~~ 601619

FGB/MD

3rd July, 1978.

Mr. A. Lewicki,
Lewicki Ltd.,
Spollanstown,
Tullamore,
Co. Offaly.

Dear Mr. Lewicki,

I enclose herewith details of an ESA tender which I think is in your field. I notice that it asks only that the Company will be capable of manufacture and test in the future.

Is there any possibility of a joint Lewicki Germany/Ireland making a bid?

Mr. Nuti was impressed with his visit.

Yours sincerely,

F. G. Burrows

F.G. Burrows